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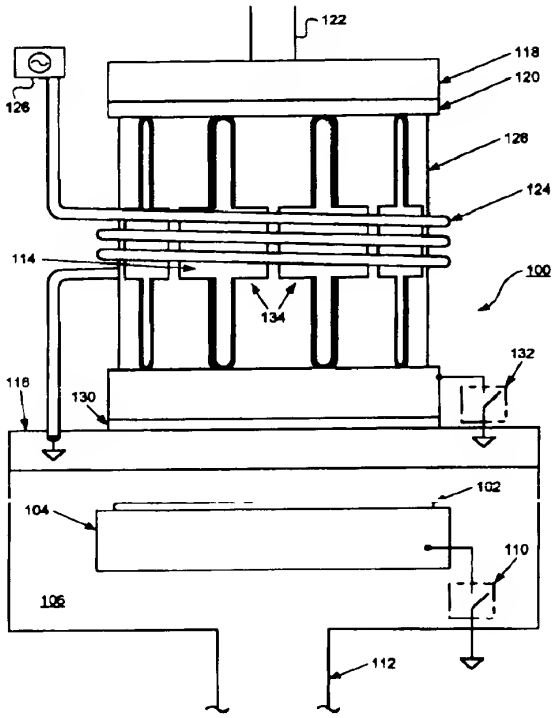
(54) Title: SYSTEMS AND METHODS FOR PLASMA ENHANCED PROCESSING OF SEMICONDUCTOR WAFERS

(57) Abstract

Systems (100) and methods for processing a semiconductor wafer (102) using variable mode and/or low or no oxygen based plasmas. The modulation of the plasma potential relative to the semiconductor wafer is varied for different process steps. A capacitive shield (128) may be selectively grounded to vary the level of capacitive coupling and modulation of the plasma. Process pressures, gases and power level may also be modified for different process steps. Plasma properties may easily be tailored to specific layers and materials being processed on the surface of the wafer. Hard to remove residues are exposed to low or no oxygen based plasmas in the presence or absence of variable mode processes to assist in their removal. Variable mode processes may be adapted for: (1) removal of photoresist after high–dose ion implant, (ii) post metal etch polymer removal, (iii) via clean, and (iv) other plasma enhanced processes.



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SYSTEMS AND METHODS FOR PLASMA ENHANCED PROCESSING OF SEMICONDUCTOR WAFERS

BACKGROUND

1. Field of the Invention

The field of the present invention relates in general to semiconductor processing. More particularly, the field of the invention relates to systems and methods for plasma enhanced processing of semiconductor wafers.

2. Background

During computer chip manufacturing, various materials are deposited onto a silicon wafer to convert the silicon wafer into a functional integrated circuit device. For instance, a bare silicon wafer may be masked with materials such as silica (silicon oxide or oxide), silicon nitride, and photoresist to protect areas on the wafer during different process steps. Subsequent to various processing steps, materials need to be removed from the surface of the wafer. Aggressive plasma enhanced processing may be desired to remove material quickly and completely, but may expose the wafer to damage.

While such difficulties may be encountered in a variety of processes, the removal of photoresist after high-dose ion implant is illustrative. Photoresist is exposed to a number of process steps that change the nature and physical qualities of the photoresist during the time that it is present on a wafer. A simplified discussion of how a semiconductor gate oxide device is formed illustrates how photoresist is used and how its characteristics are changed during use.

To form a semiconductor gate oxide device, a thick layer of oxide is usually grown on the surface of the silicon wafer. Photoresist is spun onto the oxide layer and patterned using ultraviolet light and a patterning mask, and the photoresist is subsequently developed to provide protected oxide areas and unprotected oxide areas. In a commercial process, the photoresist is developed rapidly, which usually traps some of the solvent in which the photoresist was suspended below the cured surface.

After developing the patterned photoresist, oxide is removed from the unprotected areas using reactive ion etching, for example. Once the desired oxide pattern is established, metal species such as ions, free radicals, other energetic species, or other metal atoms are implanted into silicon underlying the patterned oxide to form the gate in the semiconductor device. This process is often referred to as high-dose ion implant. Metal species are driven

through the oxide and into the silicon to a desired concentration and depth using a selected dose of metal species and high energy, and these species are also unavoidably driven into the photoresist during this process. It has been theorized that these species modify the photoresist by providing sufficient energy to drive hydrogen out of the photoresist and form double- and triple-bonded carbon atoms in the surface layer of the photoresist, creating a hardened crust and making the photoresist difficult to remove.

To complete the semiconductor gate oxide device, the contacts of the device are metalized, and the photoresist is removed from the wafer. It is highly desirable to remove the photoresist with high selectivity and minimal disturbance to the Si, SiO_2, Si_3N_4, metal, and other structural and/or masking materials present on the wafer so that device performance and reliability are ensured and so that further processing of the wafer remains uncomplicated by the resist strip. However, photoresist usually becomes very difficult to remove as a result of the numerous processing steps to which it is exposed. A number of methods have been developed in an attempt to remove this hardened and changed photoresist.

One method of removing photoresist (stripping) is a wet-chemical method as exemplified by Japanese patent application JP 55064233. In this method, a wafer having a photoresist layer is washed with a chlorinated aliphatic hydrocarbon and lower alkanol. The wafer must be washed and dried after stripping the photoresist with the chlorinated hydrocarbon and alcohol mixture, which increases the number of steps required to process wafers and consequently increases the time required to process wafers.

Another method of stripping photoresist from a wafer is a dry method that utilizes the reactive species created in a dry plasma to react with photoresist and strip it from the surface of the wafer. In a commonly-used commercial process, photoresist is removed in two steps. First, a plasma of oxygen and forming gas (a nonexplosive mixture of nitrogen and hydrogen gases) is created, and the plasma products are passed over the photoresist layer on the wafer at a temperature of approximately 150°C for approximately 5-20 minutes to remove the layer of crust from the surface. This step usually produces only partial removal of the crust. After this first step, a plasma formed from oxygen or a mixture of oxygen and nitrogen is passed over the wafer for 1-2 minutes at a temperature of approximately 250°C to remove the remaining photoresist.

Conventional plasma systems designed to minimize damage to the wafer rely

primarily on oxygen atoms and other disassociated neutral species to remove photoresist. Typically such systems are designed so that the charged, energetic species produced by the plasma tend to recombine prior to contact with the wafer or are isolated from the wafer in order to minimize potential damage to the wafer surface. The wafer is especially sensitive to damage from charged, energetic species during the final phase of photoresist removal when the areas of the wafer previously covered by the photoresist are exposed. While reducing exposure to charged, energetic species reduces the potential for damage to the wafer, it also makes it difficult to remove the hardened crust of the resist formed from high-dose ion implant.

These other hard to remove residues formed during processing and/or photoresist striping, if left on the surface of the wafer, could cause degradation of the performance of the devices or viability of the integrated circuit and therefore should be removed. Removal of these residues can be difficult and has historically been done by immersion in wet chemical baths containing either acidic or caustic chemicals. Often such chemicals are expensive and may require special handling in use and in disposal as toxic materials.

There are some residues which are easily removed including those containing silicon, carbon and halogens which remain after polysilicon gate etch or silicon dioxide contact etch processes. However, removal of the residues and polymers from the surfaces of the device after other processing steps have been performed is often difficult and may require such aggressive liquid treatments that materials on the surfaces of the device may also be etched or undesirable contaminants may be left on the wafer surface causing performance degradation. Additionally, processes either involving metal etching or etching down to a metal stop layer can leave difficult to remove residues and the surfaces of device structures can be contaminated by particulates as a result of wet chemical treatments.

An example of a residue which may be difficult to remove is that found after etch patterning of an aluminum layer. In this case the photoresist ashing process environment (almost always done immediately after etching in the same tool to avoid corrosion by atmospheric moisture) is very strongly oxidizing causing the aluminum, silicon, and carbon containing residues in the photoresist to transform to a mixture including aluminum oxide which is very resistant to chemical-attack. Another difficult to remove residue layer is usually found after etching of silicon dioxide to create vias. (Vias are the connections made from one level of metal lines to the adjacent level(s).) At the last stage of such an etching

process there can be sputtering of the metal underlying the insulating layer causing formation of metal containing residues on the sidewalls of the vias.

There are also other etching or implantation processes which create metal or silicon containing residues or other hard polymeric materials on the surface that are very hard to remove by conventional wet chemical processes. In most cases plasma-activated gas streams containing oxygen may be ineffective in ashing or making soluble such remnant materials on the wafer surface. Usually, exposure of such materials to plasma-activated gaseous streams containing oxygen, which is needed for ashing the photoresist, causes oxidation of such residues which forms even more difficult to remove materials. Other such residual materials might include some of the major dopants for semiconductors such as: boron; phosphorus; other metal layers, such as titanium – which is used for various purposes in the integrated circuit; silicon carbide; highly cross-linked or diamond-like carbon; and recently, copper has been used in integrated circuits, and whose oxides and residues need to be removed from insulator surfaces.

What is needed is a system and method for varying the properties of a plasma for variable mode processing of a semiconductor wafer. Preferably, such a system and method would allow more aggressive plasma properties to be used for selected processing steps, such as removal of hardened photoresist crust or other residues, and less aggressive plasma properties to be used for more sensitive steps including the selective removal of residues while minimizing damage to devices on the wafer. Preferably, the plasma properties may be modified using a simple switch without interrupting processing. Also what is needed is a system and method for selectively removing unwanted materials from a semiconductor wafer. Preferably, such a system and method would allow removal of difficult to remove residues while minimizing damage to devices on the wafer.

SUMMARY OF THE INVENTION

Aspects of the present invention provide a system and method for selectively varying plasma properties for processing of a semiconductor wafer. In an exemplary embodiment, the modulation of the plasma potential relative to a semiconductor wafer may be varied for different process steps. In an exemplary embodiment, a capacitive shield may be selectively grounded to vary the level of capacitive coupling and modulation of the plasma. In addition, the process pressure, gases, and power level may be modified to modify the plasma properties for different process steps. It is an advantage of these and other aspects of the

present invention that plasma properties may be substantially modified without interrupting processing. The plasma properties may be tailored to the specific layers and materials being processed on the surface of the semiconductor wafer throughout the processing cycle.

Another aspect of the present invention provides an inductively coupled plasma reactor with variable capacitive shielding to control the properties of the plasma. In one embodiment, a split or slotted capacitive shield (also referred to as a split Faraday shield) is provided between the induction coil and reactor chamber. When the shield is ungrounded relative to the induction coil (i.e., floating), a high energy plasma is formed and energetic charged species are driven toward the surface of the semiconductor wafer. This mode of operation may be used to rapidly remove layers from the surface of a semiconductor wafer. In particular, hardened layers, such as a photoresist crust, may be removed.

Grounding the shield reduces the capacitive coupling between the coil and the plasma. Without capacitive coupling driving the charged species toward the wafer surface, the plasma retracts and the density of the energetic, charged species is reduced. Nevertheless, abundant disassociated neutral species are produced in the plasma which diffuse over the wafer surface. This mode of operation may be used to remove layers of material from sensitive areas of the wafer. In particular, softer underlying layers of photoresist may be removed without damaging the semiconductor device.

Alternative mechanisms for varying capacitive shielding may also be used. For instance, a shield may be moved radially away from the reactor chamber to increase the size of the slots and decrease the level of shielding. In addition, the shield may be raised or lowered to remove all or part of the shielding. The width of the slots in the shield may also be increased or decreased by rotating an inner shield to overlap a portion of the slots. A sliding door or other mechanism may also be used. In addition, the inductor may remain shielded and an RF bias may be selectively applied to the wafer support to induce capacitive coupling. An RF bias may also be selectively applied to the shield to induce capacitive coupling.

Capacitive coupling and/or modulation of the plasma potential may also be modified in some embodiments without the use of variable capacitive shielding. For instance, a relatively high level of capacitive coupling may be provided by an inductor adjacent to a plasma generation chamber. The capacitive coupling may be reduced by raising the inductor above the chamber, so that the inductor is not aligned in a plane adjacent to the plasma. The

power to the inductor may need to be increased, so inductive fields extending radially below the inductor are sufficient to sustain the plasma. Nevertheless, capacitive coupling is reduced.

It is an advantage of these and other aspects of the present invention that the properties of a plasma may easily be modified without interrupting processing. In particular, plasmas with different properties may be used to remove different layers on a semiconductor wafer without extinguishing the plasma or requiring two different process chambers.

Of course, in alternate embodiments, two different reactors with different plasma properties could be used to remove the different layers of material. A reactor with an energetic plasma, such as a capacitive diode reactor or an unshielded or partially shielded inductively coupled reactor, could be used to remove hardened layers of material. A reactor with a lower energy plasma isolated from the semiconductor wafer surface, such as a shielded inductively coupled reactor with a charged particle filter, could be used to remove more sensitive layers.

Aspects of the present invention also provide a system and method for rapidly removing both hard and underlying soft layers of materials from the surface of a semiconductor wafer while reducing the potential for damaging underlying areas of the semiconductor wafer. The surface of the semiconductor wafer is exposed to charged, energetic species from a plasma to remove hardened layers, such as a photoresist crust hardened from high-dose ion implant. After the hardened layers are removed, modulation of the plasma potential relative to the wafer is reduced which, in turn, reduces bombardment of the wafer by charged, energetic species. In addition, the density of charged species may be reduced. The softer underlying layer of material is removed in large part by reactions with disassociated neutral species which diffuse over the wafer rather than by high energy bombardment with charged species.

Aspects of the invention also provide a system and method for rapidly removing residues and other layers using reactive species with little or no oxygen, whether or not used in combination with a variable mode plasma. One embodiment of the invention includes using reactive species from a plasma source to facilitate the removal of residues or hard to remove layer(s) remaining after metal etching on a silicon wafer, where the gases employed in creating the plasma include little or no oxygen. This includes flowing a gaseous mixture with little or no oxygen to a plasma source where reactive species are created which then

flow to a semiconductor wafer causing volatile or soluble species to be formed from the metal-containing residues on the semiconductor wafer. In this embodiment the oxygen flow is less than or equal to 2% of the total gas flow (and may be zero), or less than one third of the flow of hydrogen (hydrogen containing, and/or other reducing gases), whichever is less. The flow of the hydrogen, hydrogen-containing gases, and/or other reducing gases, comprises greater than 2% of the total gas flow. The hydrogen may be in molecular form as H_2 or other hydrogen containing gases such as methane or other hydrocarbons, ammonia or gaseous amines, water vapor or alcohols. These gases produce reactive species in the plasma which, when caused to flow to the wafer, perform selective removal (or facilitate such removal in succeeding steps) of residues which may not be removed were oxygen to be a larger component of the mixture. The reducing nature of the reactive species in this case tends to disfavor the creation of metallic oxides which are resistant to solution in water rinses. (Examples of critical layers on a wafer surface which might need to be preserved from erosion or damage might include anti-reflective coating layers (ARC) or barrier layers such as titanium nitride or titanium.)

Suitable plasma sources useful in embodiments of the invention include, but are not limited to, an inductively coupled plasma source which may or may not employ a partial electrostatic shield (Faraday shield), as described in U.S. patent no. 5,534,231, downstream-type plasma-source based tools such as are commonly used for ashing photoresist, which employ a non-resonant type (waveguide based) of microwave (typically 2.45 GHz) plasma source, a resonant cavity type microwave plasma source (Evenson), or other types commonly used for plasma-based processes including RF capacitively coupled sources, a resonant microwave based source, possibly including so-called "ECR" sources, as well as UHF sources which use antenna(e) as launchers of electromagnetic energy with frequency at or above 80 MHz into the plasma.

One exemplary embodiment of the invention includes a method and system for removal of difficult residues such as those formed after the etching of aluminum, or residues formed after the resist ashing following aluminum etching. In this embodiment a processing step is performed in which a combination of hydrogen and carbon tetrafluoride gases (but with substantially no oxygen) is injected into an inductively coupled plasma source with a partial Faraday shield to form neutral and charged species to which the wafer is exposed. The wafer is held at relatively low temperature (below 100°Celsius), causing attack (leading

to removal during the water rinse following processing) of the metal containing residues while leaving the critical material layers on the surface of the wafer substantially unharmed. Such treatment provides a slight degree of energetic ion bombardment (of the order or less than 80 microamperes/square centimeter) to help destroy chemical and physical bonds of the residues to the wafer surface.

In other embodiments of the invention, the residue removal process or process step or steps facilitating the removal of such residues comprise a subset of the totality of process steps carried out sequentially in the same processing system. In one aspect of these embodiments, the residue removal process is one or more of the contiguous steps of the total process such that there is no inactive interval between steps. Other steps in the total process may employ substantial amounts of oxygen gas fed to the plasma source in order to cause different effects on the materials exposed on the wafer. These steps would not substantially interfere with the reducing step in the process wherein there is little or no oxygen employed. In yet another aspect of the invention, residual oxygen from steps preceding low/no oxygen step(s) is substantially pumped out of the chamber prior to these step(s) allowing the process step(s) to avoid residual oxygen and/or its products.

In other embodiments of the invention processing steps may be done in non-contiguous time steps such that there is a time interval between steps, or other steps are done in a separate reactor chamber in the same processing system.

Still other embodiments of the invention include the use of hydrogen or hydrogen containing gases and/or halogenated gases, with substantially no oxygen, as principal constituent(s) to reduce (or otherwise react with) residues and polymers on a wafer for post-treatment following a dielectric etching step called "via" etch. In these embodiments, the residue removal process may be done prior to photoresist ashing in a photoresist ashing tool or an etching tool. Hydrogen containing gases useful in these embodiments include but are not limited to hydrocarbons, ammonia, water vapor or alcohols or mixtures of hydrogen in inert gases such as noble gases or nitrogen, partially fluorinated hydrocarbons, difluoromethane (CH_2F_2), other fluorocarbons (such as CF_4, C_2F_6, ...), SF_6, NF_3 or F_2 or mixtures of other halogenated gases such as Freon gases. Very small amounts of oxygen may also be used, of the order of two percent or less of the total gas flow to none at all or any amount within this range.

The ions from the plasma source are typically important in this process since they

help promote the chemical reaction of the neutral activated species with the residues. In one embodiment a source of RF power is applied to the wafer holding pedestal, or other means to capacitively couple RF energy into the plasma, to cause a sheath to be adjacent to the wafer surface such that as the ions flow towards the wafer they accelerate to the wafer surface. In this embodiment the plasma source may be separated from the wafer yet be close enough that the ions flow to the wafer in sufficient quantity to help promote chemical reactions with residue on the wafer.

In other embodiments of the invention where residues are to be removed which do not require ion bombardment, the source region and wafer processing region may be distinct and separated by a distance of up to 50 centimeters. Typically the residue or polymer removal processes in these embodiments are predominantly isotropic processes wherein sputtering and ion-assisted etching processes may be present but are not the dominant mechanisms. The etching or alteration of materials on the wafer surface in these embodiments is mainly by chemical reactions of reactive neutral species produced in the plasma source.

In another embodiment of the invention, a non-resonant microwave source is used to generate a plasma. In one particular embodiment, the microwave source uses an insulating cylindrical tube which is evacuated and through which flows the appropriate gas mixture in the proper pressure. The tube passes through a resonant microwave cavity or waveguide, either perpendicular to the walls of the guide or along its length. The cavity or waveguide is typically several centimeters to tens of centimeters in width or diameter for the commonly used microwave excitation frequency of 2.45 GigaHertz, but may be larger or smaller depending on the frequency of the microwave power utilized.

It is an advantage of these and other aspects of the present invention that a layer of material covered by a hardened crust may be rapidly removed from the surface of a semiconductor wafer without damaging sensitive underlying areas of the semiconductor wafer.

Aspects of the present invention also provide low oxygen based processes and/or variable mode plasma-enhanced processes adapted for: (i) removal of photoresist after high-dose ion implant; (ii) post metal etch polymer removal; (iii) via clean; and (iv) other plasma enhanced processes. In each case, modulation of the plasma potential, the process pressures and gases, and the power level and frequency may be selectively varied to allow efficient,

high throughput processing with reduced potential for damage to the semiconductor wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will become more apparent to those skilled in the art from the following detailed description in conjunction with the appended drawings in which:

Figure 1 illustrates an inductively coupled plasma reactor according to an exemplary embodiment of the present invention;

Figure 2 illustrates a circuit used to provide variable impedances in an alternate embodiment of the present invention;

Figure 3 illustrates a reactor with a microwave source for use in an alternative embodiment of the invention;

Figures 4A and 4B illustrate process steps for removal of photoresist after high-dose ion implant in accordance with exemplary embodiments of the present invention;

Figure 5 illustrates process steps for post metal etch polymer removal in accordance with an exemplary embodiment of the present invention;

Figure 6 illustrates process steps for via clean in accordance with an exemplary embodiment of the present invention;

Figure 7 is a chart depicting illustrative steps in a 5-step process in which step 4 includes a process step with substantially no oxygen to assist in residue removal;

Figure 8 is a chart depicting an embodiment of the invention useful for removing residue after a via etch. Step 1 of this process is performed substantially in the absence of oxygen;

Figure 9 is a chart depicting an embodiment of the invention in which step 1 is performed substantially in the absence of oxygen; and

Figures 10A and 10B illustrate an inductively coupled plasma reactor with a movable inductor according to an alternate embodiment of the present invention.

DESCRIPTION

Aspects of the present invention provide systems and methods for variable mode and/or low oxygen based plasma-enhanced processing of a semiconductor wafer. In particular, an exemplary embodiment of the present invention may be used to remove photoresist from a semiconductor wafer after high-dose ion implant, for post metal etch polymer removal, for via clean and for other plasma enhanced processes.

In an exemplary embodiment, a semiconductor wafer is placed in a plasma reactor for processing. In one mode, an energetic plasma is formed to produce both charged species and neutral dissociated species. Capacitive coupling is induced between the semiconductor wafer and the plasma and charged species are driven to the surface of the wafer. The bombardment by the charged species and reaction with dissociated neutral species together provide aggressive processing which may be used, for instance, to remove the hard outer crust on photoresist after high-dose ion implant. In this mode, the peak-to-peak modulation of the plasma potential may range from about 30 volts to 100 volts, or any range subsumed therein, and forms a sheath near the wafer surface with an average direct current potential of between about 20 volts and 60 volts, or any range subsumed therein. This mode of plasma processing may be provided by using an inductively coupled plasma reactor without capacitive shielding, with partial capacitive shielding, or with capacitive shielding that is ungrounded or poorly coupled to ground. In addition, the energy of bombardment by charged species may be enhanced by applying a bias to the wafer holder.

In another mode, the capacitive coupling between the plasma and the semiconductor wafer may be decreased to reduce bombardment by charged species and isolate the plasma from the wafer surface. In this mode, processing is carried out by dissociated neutral species and reduced bombardment by charged particles. In this mode, the peak-to-peak modulation of the plasma potential may range from about 2 volts to 10 volts, or any range subsumed therein, and the average direct current potential between the plasma and the wafer may range from about 10 volts to 15 volts, or any range subsumed therein. This mode may be provided by using an inductively coupled plasma reactor with a desired level of capacitive shielding.

By varying the amount of capacitive shielding and/or the effective coupling of the shield to ground, the modulation of the plasma potential relative to the wafer may be varied from a very low level of from a few volts to as high as 100 volts or more with effectively no shielding, or any range subsumed therein.

The foregoing techniques allow the plasma potential relative to the wafer surface to be carefully controlled and varied for different process steps. In addition, the processing pressure and gases and power level and frequency may be selectively varied along with the plasma potential to tailor the plasma properties to specific process steps without interrupting processing.

While an exemplary embodiment of the present invention is described below with

reference to particular plasma reactor configurations and processes, it will be readily apparent that other configurations and processes may be used in conjunction with aspects of the present invention. Descriptions of additional exemplary reactor configurations and processes which may be used in conjunction with aspects of the present invention are provided in U.S. Patent 5,534,231, U.S. Patent 5,234,529, U.S. Patent Application Serial No. 08/340,696 entitled "Inductive Plasma Reactor" filed November 15, 1994 and assigned to the assignee of the present application, U.S. Patent Application Serial No. 08/811,893 entitled "ICP Reactor Having a Conically-Shaped Plasma-Generating Section" filed March 5, 1997 and assigned to the assignee of the present invention, and U.S. Patent Application Serial No. 08/590,228 entitled "Hydrocarbon-Enhanced Dry Stripping of Photoresist" filed November January 23, 1996 and assigned to the assignee of the present application, each of which is incorporated herein by reference in its entirety. Additionally, other reactors which may be used include any other ion-activated or reactive ion etching type reactors such as are commonly used for anisotropic etching, plasma reactors such as the Aspen ICPsm inductively/capacitively coupled RF plasma reactor (Luo et al., U.S. Patent Application Serial No. 60/067,919, dated 11/17/97), which is incorporated herein by reference in its entirety. In particular, to enhance throughput and reduce redundancy of components in a commercial embodiment, dual wafer, dual plasma generation chamber configurations as described in U.S. Patent Application Serial Nos. 08/340,696, 08/811,893 and 08/590,228 may be used.

Figure 1 illustrates an inductively coupled plasma reactor system 100 used in an exemplary embodiment of the present invention. Referring to Figure 1, a semiconductor wafer 102 to be processed is placed on an aluminum support 104 in processing chamber 106. Support 104 may be heated or cooled by a heating or cooling system (not shown) to heat or cool wafers for processing. Gases are exhausted from the system through exhaust outlet 112. The support 104 rests on a ceramic stand (not shown) which is slotted to allow gas to escape through outlet 112.

Support 104 may be selectively coupled to ground through switch 110. When the switch is closed, charged particles can be driven to ground through semiconductor wafer 102 and support 104. Thus, when support 104 is grounded, bombardment by charged particles is enhanced. Therefore, switch 110 is typically closed when higher levels of ion bombardment are being used to etch wafer 102. When switch 110 is open, the potential of the support and

wafer tend to float at values near the potential of the plasma and ion bombardment is reduced. Therefore, switch 110 is typically open when neutral species and lower levels of bombardment are used to process sensitive areas of the wafer surface. In an exemplary embodiment, switch 110 is a vacuum switch relay to ground which allows the support to be quickly and easily switched between grounded and ungrounded states. In alternative embodiments, support 104 may be selectively coupled to an RF bias to accelerate ions toward the wafer for enhanced processing. See, e.g., U.S. Patent 5,534,231.

A plasma generation chamber 114 is situated above the processing chamber 106. The top plate 116 of the processing chamber 106 provides a common ground for the components of the plasma generation chamber, and comprises a conductive material such as aluminum or the like. The walls of the plasma generation chamber are made of a nonconductive material such as quartz or alumina and have a thickness of approximately 4 to 6 mm. The generation chamber walls are fixed at their base to the top plate 116 of the processing chamber. The top lid 118 of the plasma generation chamber can be aluminum or similar conductive material or can be the same material as the generation chamber walls. An o-ring seal 120 is compressed between top lid 118 and the plasma generation chamber walls to provide a vacuum seal. A gas inlet 122 is provided through top lid 118 to provide gases into plasma generation chamber 114.

An inductor adjacent to the plasma generation chamber, such as induction coil 124, provides power into the plasma generation chamber. In an exemplary embodiment induction coil 124 is a helical coil of copper tubing with three turns encircling the plasma generation chamber. Other inductor configurations with a different size, number of turns or in a different shape, such as a conical or pancake shape, may also be used. Induction coil 124 is connected to a radio frequency (RF) source 126 through an impedance match network or transformer (not shown). Inductively-coupled RF power is typically supplied to the reactor at one of the Industry, Scientific, Medical (ISM) standard frequencies of 13.56, 27.12, 40.68 MHz, or other harmonics of the 13.56 MHz ISM standard frequency. Usually the power is supplied to the coils through an impedance match network or transformer at a frequency in the range from 1 to 27 MHz, although lower frequencies may be used to prevent ion drive-in into the wafer being processed. RF energy is typically applied to the induction coil at a power of between about 900 and 3,000 watts, or any range subsumed therein.

A split Faraday shield 128 is provided between the induction coil 124 and the plasma

generation chamber 114. The bottom of the split Faraday shield 128 sits on an insulating ring 130 which may be used to electrically isolate the shield from the top plate 116 of the processing chamber. Compressed o-ring seals (not shown) are used to provide a vacuum seal. A switch 132 selectively couples the shield to the ground potential provided by the top plate 116.

When the shield is ungrounded, induction coil 124 inductively and capacitively couples power into the plasma generation chamber 114. The inductive coupling tends to accelerate charged particles circumferentially in a plane substantially parallel to the semiconductor wafer. The capacitive coupling modulates the plasma and drives charged particles perpendicularly toward the semiconductor wafer. In addition, the plasma produces neutral dissociated species which diffuse over the semiconductor wafer surface.

When the shield is grounded, it substantially reduces capacitive coupling between the coil and the plasma. While capacitive coupling is reduced, there is still some capacitive coupling through slots 134 formed in the shield. The reduction in capacitive coupling, in turn, reduces the modulation of the plasma potential and the bombardment of the semiconductor wafer by charged particles. Neutral activated species continue to be produced and flow over the wafer surface.

The number and size of the slots formed in the Faraday shield may be varied to change the level of capacitive coupling. In an exemplary embodiment, the Faraday shield 128 forms slots which are narrow, about 1 cm wide, along the length of the Faraday shield both above and below the coil. However, the slots are much wider in the region adjacent to the turns of the coil. In this region, the width of the slots is typically in the range of from about 2 centimeters to as wide as about 90% of the distance between the slots from center to center, or any range subsumed therein. The region of the Faraday shield forming the wider slots is generally aligned transverse to the turns of the helical coil, extending from about 0.5 centimeter to several centimeters below the turns of the coil to about 0.5 centimeter to several centimeters above the turns of the coil. In an exemplary embodiment, for use with 200 mm silicon wafers, the diameter of the Faraday shield is about 200 mm with slots about 80 mm in distance from one another from center to center. In this embodiment the width of the slots in the region of the Faraday shield adjacent to the turns of the coil is about 6 cm to 6.5 cm.

The purpose of widening the slots in the region near the induction coil is to permit a

desired level of capacitive coupling of the coil to the plasma even when the Faraday shield is grounded, thereby enhancing the energy transfer to electrons in this region and increasing the rates of ionization and production of excited species in the plasma chamber near the coil. This also serves to drive some RF current through the plasma (on the order of Amperes of current at 13.56 MHz) and modulate the plasma potential to some degree (some tens of volts at 13.56 MHz). However, the modulation of the plasma potential is not sufficient to cause the plasma to diffuse out of the plasma generation chamber and into the process chamber as long as the Faraday shield is grounded and able to serve as an RF anode to receive RF currents driven into the plasma by capacitive coupling from the induction coil.

If the Faraday shield is poorly coupled to ground and thereby floats electrically (e.g., with switch 132 open), however, the RF currents coming from the coil into the plasma by capacitive coupling cannot easily return to ground through the Faraday shield and must flow elsewhere to grounded surfaces. Such surfaces include support 104 and the walls of the processing chamber. In this case, the plasma expands sufficiently to extend out of the plasma chamber and cover the region above the wafer. A relatively narrow (order of magnitude 5 mm) dark space sheath is formed between the plasma and the wafer. Ions from the plasma accelerate across the sheath and bombard the wafer.

Switch 132 is used to selectively couple the Faraday shield 128 to the ground potential provided by top plate 116. When switch 132 is open, the potential of the Faraday shield tends to float and substantial capacitive coupling from the induction coil penetrates the Faraday shield. Therefore, switch 132 is typically open when higher levels of ion bombardment are desired for etching wafer 102. When switch 132 is closed, the Faraday shield is grounded which substantially reduces capacitive coupling from the induction coil to the plasma. Therefore, switch 132 is typically closed when neutral species are used with lower levels of bombardment to process sensitive areas of the wafer surface. In an exemplary embodiment, switch 132 is a vacuum switch relay to ground which allows the Faraday shield to be quickly and easily switched between grounded and ungrounded states.

Figure 2 illustrates a sample circuit which may be used to provide switches 110 and 132 in alternate embodiments of the present invention. Switch 110 may be formed by providing a circuit with a variable impedance between the support 104 and a ground potential. The switch is open when the circuit is tuned to provide a high impedance of the support to ground at the frequency of excitation. The variable impedance may be provided

by a series LC circuit, as shown in Figure 2, inserted between the support and a ground potential. The capacitance C is provided by a variable capacitor to allow the impedance of the circuit to be varied. The capacitance C is selected taking into account stray capacitance, C_{stray}, between the aluminum block and the other elements of the plasma reactor chamber. When a high impedance is desired, the variable capacitor is tuned so the circuit provides an effective inductance in parallel resonance with the stray capacitance, C_{stray}, at the frequency of excitation. When a low impedance is desired, the variable capacitor is tuned to be in series resonance with inductance L at the frequency of excitation. For RF power of between about 500 to 1,500 watts at 13.56 MHz, values for inductance L may range from about 0.1 to 2.0 microhenry and the value for capacitance C may be adjustable up to about 50 to 1,000 picofarads.

Switch 132 may be formed by providing a similar series LC circuit with a variable impedance between the Faraday shield 128 and ground. The capacitor is variable, and the capacitance is selected taking into account stray capacitance, C_{stray}, between the Faraday shield and other elements of the reactor. As described above, a high or low impedance may be provided by tuning the circuit to parallel resonance with C_{stray} for high impedance and to series resonance for low impedance.

Figure 3 depicts another embodiment of a processing chamber suitable for use with embodiments of the invention. Processing system 300 includes microwave power source 302. Suitable microwave power sources include but are not limited to a magnetron or a klystron. Microwave power conduit 304 can be a waveguide or coaxial cable. Insulating tube 306 passes through a microwave cavity 305 or the properly terminated end of power conduit 304, then through the charged particle filter 308, makes right angle or large angle bends 310 and passes into chamber 312. During operation of processing system 300, gas is injected into insulating tube 306 and the density of gas in the plasma is reduced as ionization takes place as the gas passes through charged particle filter 308. In one aspect of the embodiment depicted in Figure 3, bends 310 in insulating tube 306 reduce the charged particle content. Optional baffles or grids 314 are used to further reduce the charged particle content of the gas stream coming out of insulating tube 306. Reducing the charged particle content is important in some photoresist removal processes as it reduces the levels of alkali metals from the ash of the photoresist that are driven into the silicon oxide underlying the photoresist. Exhaust 316 in chamber 312 is connected to vacuum pumping equipment (not

shown) to exhaust reacted gases. Optional heat lamps 318 can be placed in chamber 312 to heat wafer 320 if desired.

Exemplary parameters for processing a semiconductor wafer in the reactor of Figure 1 in accordance with aspects of the invention will now be described. Initially, the chamber is at a pressure of about 3-10 Torr. Any processed wafer remaining in the chamber from previous processing is removed and a new wafer is placed on support 104. A robot and load lock mechanism (not shown) such as that provided by the Aspen™ system available from Mattson Technology, Inc. are used to load and unload the semiconductor wafers. After the load lock door is closed, the chamber is evacuated to the desired process pressure and process gases are flowed through inlet 122 into plasma generation chamber 114. The wafer is allowed to heat up to the desired processing temperature and gas flows are stabilized during an initial period of from several to about 10 seconds.

Typically, the gas combinations employed for photoresist removal include: oxygen, carbon tetrafluoride (or other fluorocarbon or partially fluorinated hydrocarbon) and hydrogen gas (which may be provided in a dilute mixture in an inert gas such as nitrogen or argon) or hydrogen containing gases such as C_4H_{10} or CH_3OH or H_2O. The relative flows of the different gases range from hundreds of SCCM (standard cubic centimeters per minute) to ten thousand SCCM for oxygen; from five SCCM to one thousand SCCM for fluorocarbon; and from ten SCCM to five thousand SCCM of hydrogen diluted in inert gas. The total pressure of the gas ranges from a few hundred milliTorr to as much as several Torr.

In one exemplary embodiment the initial pressure is approximately 500-700 milliTorr and the flows are: oxygen at about 1,500 SCCM, CF_4 at about 90 SCCM, and hydrogen 4% in nitrogen at about 1,500 SCCM. The support 104 is kept at a temperature of less than 100 degrees Celsius, with about 85 degrees Celsius being typical. Alternate process parameters are described further below and in U.S. Patent Application Serial No. 08/590,228, which is incorporated herein by reference.

Initially, switch 132 is open and the Faraday shield is ungrounded. After gas flows and temperatures are stabilized, RF power at 13.56 MHz is provided to induction coil 124 and the plasma is ignited in plasma generation chamber 114. The plasma produces charged particles and neutral species. The plasma generated by the induction electric field couples capacitively to the Faraday shield through the insulating vessel and picks up some fraction of the RF electric current which has been coupled from coil 124 to the Faraday shield. This

causes the electrical potential of the plasma to be modulated at the RF frequency of the current in the coil. The plasma then conducts the current which it has picked up to grounded surfaces, such as the walls of the processing chamber and support 104 which holds the semiconductor wafer. The conduction of the RF current to the wafer which rests on support 104 causes current to pass also through the wafer and sets up a plasma sheath above the wafer. This sheath serves to accelerate positively charged ions toward the photoresist crust on the wafer surface. The bombardment by these ions is an important factor in various etching processes, because it promotes the breaking of bonds for materials to be etched on the wafer surface.

The system is operated in this high energy mode for between about 1 to 5 minutes as necessary to etch away the hard photoresist crust, with 3 to 3 1/2 minutes being typical. Empirical data for a given process may be used to determine the time necessary for sufficiently etching the crust. Alternatively an optical end point detection method may be used. The photon emissions from the surface of the wafer change as the crust is etched away. Therefore an optical sensor, such as an optical pyrometer, may be used to determine how much of the crust has been removed. Typically, after the crust has been removed, the photoresist continues to be etched in the high energy mode for a period of about 30 seconds. This overetching ensures that all of the crust has been removed and also begins removing the soft underlying resist. In sensitive processes, the high energy mode may be stopped earlier to ensure that the photoresist is not prematurely etched away on some parts of the wafer leaving the bare wafer exposed to high energy ion bombardment.

When the ion bombardment phase of the process is concluded and remaining materials or residues are to be processed in a less aggressive manner, the Faraday shield switch 132 is closed which causes the Faraday shield to be grounded. This in turn removes the RF current from the Faraday shield, and prevents this current from conducting into the plasma. The lack of RF current conducting through the plasma causes the plasma to retract from the processing chamber back into the plasma generation chamber. This substantially reduces the conduction of current to the wafer and hence the sheath which accelerates the ions toward the surface of the wafer. Therefore, the energy of ions bombarding the wafer is significantly reduced and the system operates in a low energy mode. In addition, switch 110 may be opened to further reduce current flow to the wafer. This provides a less aggressive plasma process for removing photoresist from the wafer, because energetic ion

bombardment is substantially eliminated. Reactive neutral species, on the other hand, continue to be produced and flow to the surface of the semiconductor surface. The neutral species readily react with and remove the soft photoresist without high energy ion bombardment.

During the low energy mode, the process gases may be changed slightly to reduce aggressive fluorine containing compounds and increase neutral oxygen species. For instance, the pressure may be increased to approximately 1 to 1.1 Torr which reduces ion density and the flows may be modified to about: oxygen at about 3,000 SCCM, CF_4 at about 60 SCCM, and hydrogen 4% in nitrogen at about 1,500 SCCM.

The system may be operated in the low energy mode until all of the soft underlying resist is removed. In addition, an overetch may be performed to ensure that all of the photoresist is removed. Even though the surface of the wafer is exposed during overetch, the potential for damage is reduced due to the low level of ion bombardment. In a typical process, the soft photoresist is removed in about a minute and about 30 seconds of overetch is performed.

After the photoresist has been removed, the RF power is turned off and the process gases are turned off. Nitrogen gas is flowed to purge the chamber and the pressure is raised to about 3-10 Torr. The processed wafer may then be removed and a new wafer may be placed in the chamber.

Additional exemplary processes will now be described with reference to Figures 4-6. Figures 4A and 4B illustrate process steps and parameters used for low temperature removal of photoresist after high-dose ion implant (hereinafter "HDIS process"). These processes are adapted to allow fast removal of photoresist with minimum oxide loss and without causing popping on the wafer. These goals are achieved by running at low temperature (lower than the baking temperature of about 160°C) with different chemistries than typical conventional systems and by using variable mode plasma-enhanced processing.

Figure 4A illustrates an HDIS process which provides a relatively fast process, but may result in some oxide loss. During step 1, a wafer with photoresist hardened by high-dose ion implant is placed in the processing chamber. The wafer also includes thin oxide layers which are not intended to be etched away by the process. Step 1 of the process has a short duration of only about 5 seconds and is used to stabilize conditions in the processing chamber. Initially, the pressure of the processing chamber is about 8 Torr. Gases are flowed

at the following rates: oxygen (O_2) at about 5,000 SCCM, forming gas of 4% hydrogen (H_2) in argon (Ar) at about 1,400 SCCM and CF_4 at about 90 SCCM. The temperature of support 104 is maintained at about 85 degrees Celsius throughout the process. The Faraday shield is ungrounded and switch 132 is open. RF power is not applied during this step.

During step 2, the pressure is reduced to about 1.1 Torr and gases are flowed at the following rates: oxygen (O_2) at about 1,500 SCCM, forming gas of 4% hydrogen (H_2) in argon (Ar) at about 1,400 SCCM and CF_4 at about 90 SCCM. The Faraday shield remains ungrounded. After a delay of about 10 seconds after the start of step 2, RF power is applied to induction coil 124 at a frequency of 13.56 MHz and a power level of about 800 watts. During this step, an energetic plasma is ignited and the hardened photoresist crust is etched by ion bombardment. The plasma extends into the processing chamber and forms a sheath at the wafer surface. Step 2 has an overall duration of about 85 seconds.

During step 3, the pressure is reduced to about 0.6 Torr and gases are flowed at the following rates: oxygen (O_2) at about 1,500 SCCM, forming gas of 4% hydrogen (H_2) in argon (Ar) at about 1,400 SCCM and CF_4 at about 90 SCCM. Switch 132 is closed and the Faraday shield is grounded. At the same time, RF power is increased to a power level of about 1,100 watts. During this step, the plasma retracts into the plasma generation chamber, which reduces energetic ion bombardment even though pressure is reduced and power is increased. The reduced pressure and increased power cause the plasma to produce abundant dissociated neutral species which diffuse over the wafer surface, while the Faraday shield reduces capacitive coupling and ion bombardment. Step 3 has an overall duration of about 75 seconds.

During step 4, the RF power is turned off and pressure is raised to about 8 Torr. Oxygen is (O_2) is flowed at about 5,000 SCCM. The other gases are turned off. Step 4 has a duration of about 5 seconds, after which the processed wafer is removed. The overall process has a duration of about 170 seconds. This results in a throughput of about 15 wafers per hour in a single wafer reactor and about 35 wafers per hour in a dual wafer reactor.

Figure 4B illustrates an HDIS process which is slightly slower than the process described above, but results in almost no oxide loss. During step 1, a wafer with photoresist hardened by high-dose ion implant is placed in the processing chamber. The wafer also includes thin oxide layers which are not intended to be etched away by the process. Step 1 of the process has a short duration of only about 5 seconds and is used to stabilize conditions

in the processing chamber. Initially, the pressure of the processing chamber is about 8 Torr. Gases are flowed at the following rates: oxygen (O_2) at about 2,300 SCCM, forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 600 SCCM and CF_4 at about 90 SCCM. The temperature of support 104 is maintained at about 85 degrees Celsius throughout the process. The Faraday shield is ungrounded and switch 132 is open. RF power is not applied during this step.

During step 2, the pressure is reduced to about 1.1 Torr and gases are flowed at the following rates: oxygen (O_2) at about 2,300 SCCM, forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 600 SCCM and CF_4 at about 90 SCCM. The Faraday shield remains ungrounded. After a delay of about 10 seconds, RF power is applied to induction coil 124 at a frequency of 13.56 MHz and a power level of about 1,000 watts. During this step, an energetic plasma is ignited and the hardened photoresist crust is etched by ion bombardment. The plasma extends into the processing chamber and forms a sheath at the wafer surface. Step 2 has an overall duration of about 115 seconds.

During step 3, the pressure is reduced to about 0.6 Torr and gases are flowed at the following rates: oxygen (O_2) at about 2,300 SCCM, forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 600 SCCM and CF_4 at about 90 SCCM. Switch 132 is closed and the Faraday shield is grounded. At the same time, RF power is increased to a power level of about 1,200 watts. During this step, the plasma retracts into the plasma generation chamber, which reduces energetic ion bombardment even though pressure is reduced and power is increased. The reduced pressure and increased power cause the plasma to produce abundant dissociated neutral species which diffuse over the wafer surface, while the Faraday shield reduces capacitive coupling and ion bombardment. Step 3 has an overall duration of about 75 seconds.

During step 4, the RF power is turned off and pressure is raised to about 8 Torr. Oxygen (O_2) is flowed at about 5,000 SCCM. The other gases are turned off. Step 4 has a duration of about 5 seconds, after which the processed wafer is removed. The overall process has a duration of about 200 seconds. This results in a throughput of about 12 wafers per hour in a single wafer reactor and about 30 wafers per hour in a dual wafer reactor.

Figure 5 illustrates process steps and parameters used for post metal etch polymer removal. This process is adapted for removing sidewall polymer that remains after metal etch and dry strip of photoresist. Metal etch processes are anisotropic due to the generation

of sidewall material (referred to as polymer). This material is composed of carbon, chlorine, aluminum, and may also contain boron oxides and chlorides from the BC13 etch gas additive. Typical integrated ash processes are developed with the goal of eliminating corrosion of the aluminum lines due to the presence of chlorine in the polymer. These processes have good corrosion resistance yet poor polymer removal. The process described below removes the polymer and eliminates the need for organic solvents or acidic treatments which are commonly used for the same purpose. By going to an all-dry process with only a de-ionized water rinse, significant cost savings can be realized.

During step 1, a wafer is placed in the processing chamber. Step 1 of the process has a short duration of only about 6 seconds and is used to stabilize conditions in the processing chamber. Initially, the pressure of the processing chamber is about 1.1 Torr. Gases are flowed at the following rates: forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 500 SCCM and CF_4 at about 300 SCCM. It should be noted that oxygen gas is not flowed to the chamber during step 1. TiN or Ti barrier and ARC layers are susceptible to attack in the presence of fluorine and oxygen, if exposure applies in the first step. The temperature of support 104 is maintained at about 75 degrees Celsius throughout the process. The etch induced polymer material apparently oxidizes at higher temperatures (e.g., above 100°C), rendering the polymer more difficult to remove. The Faraday shield is ungrounded and switch 132 is open. After a delay of about 4 seconds RF power is applied at a frequency of 13.56 MHz and a power level of about 850 watts. During this step, an energetic plasma is ignited and established. The plasma extends into the processing chamber and forms a sheath at the wafer surface.

During step 2, the pressure is increased to about 2.5 Torr and gases are flowed at the following rates: forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 1,900 SCCM and CF_4 at about 300 SCCM. The Faraday shield remains ungrounded. RF power is lowered to about 650 watts. During this step, polymer is etched by ion bombardment. Step 2 has an overall duration of about 20 seconds.

During step 3, the pressure is reduced to about 0.6 Torr and gases are flowed at the following rates: oxygen (O_2) at about 3,000 SCCM, and CF_4 at about 150 SCCM. Faraday switch 132 is closed and the Faraday shield is grounded. At the same time, RF power is increased to a power level of about 1,150 watts. During this step, the plasma retracts into the plasma generation chamber, which reduces energetic ion bombardment even though

pressure is reduced and power is increased. The reduced pressure and increased power cause the plasma to produce abundant dissociated neutral species which diffuse over the wafer surface for bulk resist strip, while the Faraday shield reduces capacitive coupling and ion bombardment. Step 3 has an overall duration of about 46 seconds.

During step 4, the pressure is raised to about 2.5 Torr and gases are flowed at the following rates: forming gas of 4% hydrogen (H_2) in nitrogen (N_2) at about 1,900 SCCM and CF_4 at about 300 SCCM. The Faraday shield is ungrounded. At the same time, RF power is decreased to a power level of about 650 watts. During this step, residue is removed by ion bombardment. The plasma extends into the processing chamber and forms a sheath at the wafer surface. Step 4 has an overall duration of 30 seconds.

During step 5, pressure is decreased to about 1.1 Torr. Oxygen is (O_2) is flowed at about 3,500 SCCM. The other gases are turned off and the Faraday shield is ungrounded. Step 5 has a duration of about 5 seconds, after which the processed wafer is removed. The overall process has a duration of about 107 seconds. This results in a throughput of about 25 wafers per hour in a single wafer reactor and about 50 wafers per hour in a dual wafer reactor.

Figure 6 illustrates process steps and parameters used for via veil removal. This process is adapted for removing tough via veils that are generated from oxide etch processes. The purpose of the process is to open a conductive pathway to the aluminum underlayer. This etch process is designed to remove only the oxide material under the opened mask layer. In order to provide anisotropy during the etch, polymerizing process chemistries are used in conjunction with sufficient ion bombardment to passivate the etched sidewall. Once this oxide layer is opened and cleaned, subsequent steps deposit metal contacts which allow vertical integration of devices. In this way lateral space is conserved, allowing for more densely-packed transistor layers and metal interconnect layers. Unlike typical conventional processes, the process described below removes both the bulk photoresist masking layer and the via sidewall polymer material without the use of solvents or aggressive acidic solutions. This provides significant cost savings.

In addition, the process described below is carried out at relatively low temperatures of from about 25 to 75 degrees Celsius. TiN or Ti ARC layers are susceptible to attack at higher temperatures of 250°C, but not in the 25°C to 75°C temperature range used in the current process. SOG layer attack is also seen at higher temperatures, resulting in profile

distortion of the via. In addition, the etch induced polymer material oxidizes at higher temperatures rendering the polymer more difficult to remove. If the polymer film contains aluminum due to exposure of aluminum layers during the etch process, it can be easily oxidized to Al_2O_3 rendering the film even more difficult to remove. The process described below, on the other hand, is carried out at low temperatures and is capable of yielding clean vias with only a de-ionized water rinse.

During step 1, a wafer is placed in the processing chamber. Step 1 of the process has a short duration of only about 5 seconds and is used to stabilize conditions in the processing chamber. Initially, the pressure of the processing chamber is about 8 Torr. Gases are flowed at the following rates: oxygen (O_2) at about 5,000 SCCM. The temperature of support 104 is maintained at about 25 to 70 degrees Celsius throughout the process with 25 degrees Celsius being typical. The Faraday shield is ungrounded and switch 132 is open. RF power is not applied during this step.

During step 2, the pressure is maintained at about 0.7 Torr and gases are flowed at the following rates: oxygen (O_2) at between 1,000 to 4,000 SCCM with 3,000 SCCM being typical, fluorine containing gases (CF_4 or NF_3) from 1% to 3%, with 30 SCCM of NF_3 being typical. The Faraday shield remains ungrounded. After a delay of about 10 seconds, RF power is applied to induction coil 124 at a frequency of 13.56 MHz and a power level of between 700 to 1,000 watts with 800 watts being typical. During this step, polymer is etched by ion bombardment. The plasma extends into the processing chamber and forms a sheath at the wafer surface. Step 2 has a duration of about 75 seconds.

During step 3, the RF power is turned off and pressure is raised to 8 Torr, oxygen (O_2) is flowed at 5,000 SCCM. The other gas is turned off. Step 3 has a duration of about 5 seconds after which the processed wafer is removed. The overall process has a duration of about 90 seconds. This results in a throughout of about 60 wafers per hour in a single wafer reactor and about 100 wafers per hour in a dual wafer reactor.

Exemplary parameters for processing a semiconductor wafer for residue removal in accordance with embodiments of the invention using reactor embodiments of Figures 1 and 3 will now be described. The present invention can be implemented on any reactor capable of achieving the desired process parameters and is not meant to be limited to the two reactor embodiments of Figures 1 and 3. Aspects of the invention using low or no oxygen may be used in any variety of plasma reactors and are not limited to use with variable mode plasmas

as described above.

A. Post Metal-Etch Polymer Removal

One embodiment of the invention includes a system and method suitable for the removal of residues left after etching of aluminum or other metals, or residues left after resist ashing immediately following metal etching or other metal pattern processing. The wafer to be processed is either placed in the chamber or remains in the chamber after previous processing. During step 1 of this embodiment of the invention, the wafer is held at a temperature of about 75 degrees Celsius. (This temperature may be in a range from about room temperature to as much as a few hundred degrees Celsius). This is achieved by heating a wafer support structure such as support 104 of Figure 1 or through the use of heat lamps such as those in Figure 3. The wafer is held for a 2 second interval at a chamber pressure of about 2.5 Torr and a flow rate of about 4,500 SCCM flow of N_2H_2 forming gas (typically a mixture of 5% H_2 and 95% N_2) and a flow rate of about 360 SCCM flow of CF_4. In one aspect of this embodiment, there is substantially no flow of oxygen into the chamber. Step 1 of this embodiment is performed to stabilize the conditions in the chamber – note no RF power is used. This step may be omitted if tight control over the gas pressure and flow during plasma operation is not required. Typically such control is necessary for consistent processing of wafers.

During step 2 a plasma is ignited in the chamber, and about 1,400 watts of RF power is applied. The chamber pressure and gas flow rates are maintained at about the same level as in step 1, at a pressure of about 2.5 Torr with a N_2H_2 flow rate of about 4,500 SCCM and a CF_4 flow rate of about 360 SCCM. Optionally, the plasma potential or the potential of the wafer may be modulated to cause ions from the plasma to accelerate to the wafer. This may be desired to help speed up the chemical reactions of the gases and radicals with residues and polymers on the wafer. Using the chamber depicted in Figure 1, this is achieved by opening switch 110.

In the embodiment of the invention discussed above, the gas pressures and flow rates in step 2 of this process may vary between pressures of 2.25 Torr and 2.75 Torr, or any range subsumed therein, flow rates can vary by 10% above or below the numbers stated above, or any range subsumed therein, preferably 5% above or below the number stated above.

In other embodiments of the invention, the wafer temperature may vary between 50

degrees Celsius and 200 degrees Celsius, or any range subsumed therein. In another aspect of this embodiment, if the parameters for gas pressure and/or gas flow for step 2 are varied, then about the same parameters are used in step 1 to stabilize the conditions in the chamber prior to plasma ignition.

In still other embodiments of the invention the two steps described above are part of a sequence of steps, in which substantially no oxygen is used to remove particularly stubborn residues or to remove the undesired products formed on the wafer by previous process steps.

Hydrogen containing gases that can be used in embodiments of the invention include but are not limited to hydrocarbons, ammonia, mixtures of hydrogen in inert gases such as noble gases or nitrogen. Other gases which may be used as a source for both halogen and hydrogen include but are not limited to halogenated hydrocarbons such as difluoromethane (CH_2F_2).

In still other embodiments, other additive process gases might include other fluorocarbons (such as CF_4, C_2F_6, ...), SF_6, NF_3 or F_2 or mixtures of other halogenated gases such as Freon gases. Other gases may be used in small amounts in combination with these gases, possibly including vapors such as alcohol or water vapor or CO, or others which may include some oxygen. Very small amounts of pure oxygen gas may also be used, of the order of one percent or less of the total gas flow, or none at all.

Yet another embodiment of the invention includes the use of a microwave based system such as the system depicted in Figure 3 for generating the plasma. The pressures used in this embodiment in steps 1 and 2 can vary from 10 mTorr to 10 Torr, or any range subsumed therein, preferably 100 mTorr to 2 Torr with flow rates of N_2H_2 or (other hydrogen containing gases) varying from 100 SCCM to 10,000 SCCM, or any range subsumed therein, preferably, 200 SCCM to 5,000 SCCM. The higher flows in this range are typically used in cases where hydrogen is present in a dilute mixture, such as in forming gas. The flow rate of CF_4 (or fluorine containing gas) should remain within a factor of 3 of the same proportions as in the above embodiments. Other gases which may be used as a source for both halogen and hydrogen include but are not limited to halogenated hydrocarbons such as difluoromethane (CH_2F_2). Other additive process gases might include other fluorocarbons (such as CF_4, C_2F_6, ...), SF_6, NF_3 or F_2 or mixtures of other halogenated gases such as Freon gases. The optimal pressure to use with such a microwave source will depend on the

diameter of the plasma source and the cavity modes which dominate the energy transferred to the plasma.

Other embodiments of the invention include means to cause the positive ions from the plasma to accelerate toward and bombard the wafer with enhanced energy. Suitable means include but are not limited to inducing in the plasma a potential with a significant RF component while the wafer is held on a grounded pedestal, or applying RF power to the wafer or a pedestal holding the wafer, or any other method for creation of a potential difference between the plasma and the wafer such that a sheath with an enhanced potential drop forms between the plasma and the wafer causing such ion acceleration and bombardment to take place. The level of RF power employed for this ion acceleration can range from 10 watt to 1 kilowatt or any range subsumed therein, preferably in the range of a few tens of watts to a few hundred watts for an 8 inch wafer, and the power level should scale roughly linearly with wafer area.

2. Via Etch Process

Another embodiment of the invention is useful after via etching has occurred. In this embodiment, the optional first step lasts for about 2 seconds and at a pressure of about 0.6 Torr, a flow rate of 1,500 SCCM of N_2H_2 is used and a flow rate of 100 SCCM of CF_4 is used.

In step 2 with an RF power of 1,000 watts for 40 seconds, about the same pressure and flow rates as in step 1 above are used. Optionally, a source of RF energy may be applied to the wafer or the plasma to cause a sheath at the wafer which accelerates ions into the residue on the wafer to promote the chemical reactions of the ions or active neutral species with the hard residues to convert them into forms that are easier to remove.

Still another embodiment of the invention useful after via etching has occurred includes the use of a microwave based system for generating the plasma such as the system depicted in Figure 3. The pressures used in this embodiment in steps 1 and 2 can vary from 100 mTorr to 4 Torr, or any range subsumed therein, preferably 200 mTorr to 2 Torr. In other embodiments of the invention, the flow rate of N_2 mixed with H_2, wherein the mixture of N_2 and H_2 is usually about 5% hydrogen, can vary from 300 SCCM to 2000 SCCM or any range subsumed therein, preferably 1,425 SCCM to 1,575 SCCM, and the flow rate of CF_4 can vary from 20 SCCM to 100 SCCM or any range subsumed therein, preferably 90 SCCM to 110 SCCM. In yet another embodiment of this invention, an RF bias is applied to the

wafer, through for example, the pedestal. This helps to accelerate the ions into the residue and speed up the process, particularly in the case of hardened residues.

3. Post Passivation-Etch Wafer Cleaning

Another embodiment of the invention is suitable for use after passivation-etching (otherwise known as bond pad etching) of a wafer. This embodiment may include 3 initial steps utilizing substantial amounts of oxygen in order to strip the photoresist prior to the step in which the residues are removed.

In the first step of the cleaning process with an RF power of about 1,200 watts for about 10 seconds and a pressure of about 2.5 Torr, a flow rate of about 4100 SCCM of N_2H_2 and a flow rate of about 750 SCCM of CF_4 is used. Optionally, a source of RF energy may be applied to the wafer or the plasma to cause a sheath at the wafer which accelerates ions into the residue on the wafer to promote the chemical reactions of the ions or active neutral species with the hard residues to convert them into forms that are easier to remove.

In other embodiments of the invention, the RF power may vary from 300 watts to 3000 watts or any range subsumed therein, preferably 600 watts to 1,800 watts. The pressure may vary from 200 mTorr to 4 Torr, or any range subsumed therein, preferably 500 mTorr to 3.0 Torr. The total flow rate of the two gasses may vary from 1/3 to 3 times the flow rates above or any range subsumed therein, while the relative flow rates of the two gases may vary by up to plus or minus 50%. The duration of this step may vary between 1 second and 100 seconds or any range subsumed therein, preferably 5 seconds to 15 seconds.

Still another embodiment of the invention useful after passivation-etching of a wafer includes the use of a microwave based system for generating the plasma such as the system depicted in Figure 3. The pressures of the cleaning step used in this embodiment can vary from 100 mTorr to 5 Torr, or any range subsumed therein, preferably 300 mTorr to 4 Torr and a flow rate of about 3,000 SCCM of N_2H_2 is used and a flow rate of about 400 SCCM of CF_4 is used. In other embodiments of the invention, the total flow rate of the two gasses may vary from 1/3 to 3 times the flow rates above, while the relative flow rates of the two gases may vary by a factor of two in either direction. In yet another embodiment of this invention, an RF bias is applied to the wafer, through for example, the support the wafer sits on. This helps to accelerate the ions into the residue and speed up the process, particularly in the case of hardened residues.

In other embodiments of this invention combinations of gases including hydrogen

containing gases and halogenated gases may be used in the same source chamber and processing chamber hardware for other processes including: the reduction of oxidation residues on the surface of wafers with exposed copper; the conversion of metallic residues such as cobalt, metals of the platinum group including nickel, platinum, ruthenium, rhenium, and others to more soluble forms such as halides which may be washed off the wafer in a de-ionized water rinse; making soluble many of the alkali and transition metals which may have been left on the wafer following photoresist ashing.

Figures 7-9 depict recipes for various wafer fabrications processes, which include low oxygen or no oxygen cleaning steps. Figure 4 depicts a five-step process for final passivation strip and clean. In this process, the wafer is maintained at a temperature of about 75 degrees Celsius.

The above described embodiments are exemplary only. It is understood that any variety of plasma reactors and process parameters may be used in conjunction with aspects of the present invention. For instance, high and low energy modes could be provided in two separate chambers and a semiconductor wafer could be moved between the high energy chamber and the low energy chamber for different process steps. A reactor with an energetic plasma, such as a capacitive diode reactor or an unshielded or partially shielded inductively coupled reactor, could be used to remove hardened layers of material. A reactor with a lower energy plasma isolated from the semiconductor wafer surface, such as a shielded inductively coupled reactor with a charged particle filter (see U.S. Patent Application Serial No. 08/340,696), could be used to remove sensitive layers. The wafer support in the second chamber could be hotter than in the first chamber, because problems with photoresist popping are reduced after the crust is removed (see U.S. Patent Application Serial No. 08/590,228).

In addition, other mechanisms for varying capacitive shielding and plasma modulation may be used. For instance, a Faraday shield may be moved radially away from the reactor chamber to increase the size of the slots and decrease the level of shielding. In addition, the Faraday shield may be raised or lowered to remove all or part of the shielding. The width of the slots in the Faraday shield may also be increased or decreased by rotating an inner Faraday shield to overlap a portion of the slots. A sliding door or other mechanism may also be used. An RF bias may also be selectively applied to the wafer support at varying power levels and frequencies to vary capacitive coupling and the plasma sheath

above the wafer surface. In addition, the Faraday shield may be selectively coupled to an RF bias to induce capacitive coupling.

Capacitive coupling and/or modulation of the plasma potential may also be modified in some embodiments without the use of variable capacitive shielding. Figures 10A and 10B illustrate an alternate embodiment with a movable inductor for varying capacitive coupling. Figure 10A shows a reactor 1000 with a plasma generation chamber 1010 having a non-conductive wall 1008. A wafer 1004 is placed on a support 1006 for processing. Gas is provided through inlet 1012. RF power is applied to inductor 1002 to couple power into the chamber both inductively and capacitively.

Figure 10B shows an alternate configuration of reactor 1000 for a processing mode with reduced capacitive coupling. Inductor 1002 is raised above chamber 1010 which reduces capacitive coupling. Inductive fields extending radially below inductor 1002 sustain the plasma in chamber 1010. The power applied to inductor 1002 may be increased to sustain the plasma. Nevertheless, capacitive coupling is reduced thereby providing an alternate mode of processing.

Aspects of the present invention may also be used for other plasma-enhanced processes such as low temperature de-scum and post passivation-etch photoresist stripping, although the process gases, pressures, power and temperatures may differ. For instance, for certain processes, pulsed power may be applied to the induction coil and/or wafer support. See U.S. Patent Application Serial No. 08/727,209 entitled "Apparatus and Method for Pulsed Plasma Processing of a Semiconductor Substrate" filed October 8, 1996, assigned to the assignee of the present application and incorporated herein by reference in its entirety.

While this invention has been described and illustrated with reference to particular embodiments, it will be readily apparent to those skilled in the art that the scope of the present invention is not limited to the disclosed embodiments but, on the contrary, is intended to cover numerous other modifications and equivalent arrangements which are included within the spirit and scope of the following claims.

CLAIMS

We claim:

1. A method for assisting the removal of residue from a wafer, comprising:

flowing a gas containing substantially no oxygen into a chamber containing the wafer with residue to be removed;

generating a plasma from the gas wherein the plasma includes neutral particles and ions;

flowing at least a part of the plasma over the wafer; and

forming soluble compounds on the wafer from the chemical interaction of the plasma with aluminum in the residue on the wafer.

2. The method of claim 1, wherein the gas includes a halogen containing gas.

3. The method of claim 2, wherein the gas includes a hydrogen containing gas.

4. The method of claim 3, wherein the hydrogen containing gas includes a hydrocarbon.

5. The method of claim 3, wherein the hydrogen containing gas includes ammonia.

6. The method of claim 1, comprising maintaining a chamber pressure between 2 Torr and 3 Torr.

7. The method of claim 2, wherein the halogen containing gas includes a fluorine containing gas.

8. The method of claim 7, wherein the fluorine containing gas includes a fluorocarbon.

9. The method of claim 1, wherein generating the plasma occurs a predetermined time after flowing the gas starts.

10. The method of claim 1, wherein generating the plasma includes using at least 1,000

watts of radio frequency power.

11. The method of claim 7, wherein flowing the gas includes flowing the hydrogen containing gas at a rate between 100 SCCM and 10,000 SCCM.

12. The method of claim 11, wherein flowing the gas includes flowing the fluorine containing gas at a rate between 10 SCCM and 1,000 SCCM.

13. The method of claim 7, wherein flowing the gas includes flowing the hydrogen containing gas at a rate between 1,000 SCCM and 5,000 SCCM.

14. The method of claim 13, wherein flowing the gas includes flowing the fluorine containing gas at a rate between 50 SCCM and 1,000 SCCM.

15. The method of claim 1, wherein generating the plasma includes using microwaves.

16. The method of claim 1, wherein flowing at least a part of the plasma over the wafer includes flowing ions over the wafer at a rate below 70 microamperes/cm^2.

17. The method of claim 1, comprising heating the wafer to a temperature in the range between 50 degrees Celsius and 200 degrees Celsius.

18. The method of claim 1, wherein generating the plasma occurs for a time period between 20 seconds and 60 seconds.

19. The method of claim 1, wherein generating the plasma occurs for a time period between 5 seconds and 20 seconds.

20. The method of claim 1, wherein the residue includes aluminum.

21. A method for assisting the removal of residue containing metals from a wafer, wherein the metals include aluminum, the method comprising:

flowing a gas into a chamber containing the wafer with residue to be removed, wherein the gas contains a hydrogen containing gas, a fluorine containing gas;

generating a plasma from the gas wherein the plasma includes neutral particles and ions;

flowing at least a part of the plasma over the wafer; and

forming soluble compounds on the wafer from the chemical interaction of the plasma with aluminum in the residue on the wafer.

22. The method of claim 21, wherein the gas includes no more than 2% oxygen.

23. The method of claim 21, comprising forming volatile compounds on the wafer from the chemical interaction of the plasma with metals in the residue on the wafer.

24. The method of claim 21, wherein the hydrogen containing gas includes molecular hydrogen mixed with molecular nitrogen in a ratio of 1:10 or less.

25. The method of claim 21, wherein the fluorine containing gas includes carbon tetrafluoride.

26. The method of claim 21, wherein a flow rate of the hydrogen containing gas is between 4000 SCCM and 5000 SCCM and a flow rate of the fluorine containing gas is between 320 SCCM and 400 SCCM.

27. The method of claim 21, wherein a flow rate of the hydrogen containing gas is between 1400 SCCM and 1600 SCCM and a flow rate of the fluorine containing gas is between 90 SCCM and 110 SCCM.

28. The method of claim 21, wherein a flow rate of the hydrogen containing gas is between 2000 SCCM and 8000 SCCM and a flow rate of the fluorine containing gas is between 250 SCCM and 2250 SCCM.

29. The method of claim 21, wherein flowing at least a part of the plasma over the wafer

includes flowing ions over the wafer at a rate below 70 microamperes/cm^2.

30. The method of claim 21, comprising heating the wafer to a temperature in the range between 50 degrees Celsius and 200 degrees Celsius.

31. The method of claim 21, wherein generating the plasma occurs for a time period between 20 seconds and 60 seconds.

32. The method of claim 21, wherein generating the plasma includes using microwaves.

33. A reactor system for assisting the removal of residue from a wafer, the reactor system comprising:

a reactor chamber within which a plasma is generated to produce plasma products for assisting the removal of residue from the wafer wherein the plasma products include charged particles and neutral species;

a gas inlet through which gas is provided to the reactor chamber;

means for generating the plasma, the means for generating the plasma being adjacent to the plasma;

a support for the wafer positioned inside the chamber such that the wafer on the support is exposed to at least one plasma product during processing wherein a soluble compound is formed on the wafer from the chemical interaction of the plasma with the residue on the wafer.

34. The system of claim 33, wherein the means for generating the plasma includes a microwave power source.

35. The system of claim 33, wherein the residue includes aluminum and wherein the soluble compound formed on the wafer includes aluminum.

36. The system of claim 33, comprising means for controlling the plasma potential relative to the support such that the wafer is processed in at least two modes, a first mode and a second mode.

37. The system of claim 36, wherein the gas includes no more than 2% oxygen.

38. The system of claim 36, wherein the plasma potential relative to the support in the first mode induces bombardment of the wafer by charged particles from the plasma at a desired level for processing during the first mode;

wherein the plasma potential relative to the support in the second mode is controlled to substantially reduce bombardment of the wafer by charged particles during the second mode; and

wherein the wafer is exposed to neutral species from the plasma at a desired level for processing during the second mode.

39. A plasma reactor for processing a semiconductor wafer comprising:

a reactor chamber within which a plasma is generated to produce plasma products for processing the semiconductor wafer wherein the plasma products include charged particles and neutral species;

a gas inlet through which gas is provided to the reactor chamber;

an electrode adjacent to the plasma;

a power source operatively coupled to the electrode to provide power to the plasma;

a support for the semiconductor wafer positioned such that the wafer is exposed to at least one plasma product during processing;

means for controlling the plasma potential relative to the support such that the semiconductor wafer is processed in at least two modes, a first mode and a second mode;

wherein the plasma potential relative to the support in the first mode induces bombardment of the semiconductor wafer by charged particles from the plasma at a desired level for processing during the first mode;

wherein the plasma potential relative to the support in the second mode is controlled to substantially reduce bombardment of the semiconductor wafer by charged particles during the second mode; and

wherein the semiconductor wafer is exposed to neutral species from the plasma at a desired level for processing during the second mode.

40. The reactor of claim 39, wherein:

the gas includes a hydrogen containing gas, an oxygen containing gas, and a halogen containing gas.

41. The reactor of claim 40, wherein the halogen containing gas includes fluorine.

42. The reactor of claim 40, wherein the hydrogen containing gas includes a mixture of molecular nitrogen with molecular hydrogen containing about 4% molecular hydrogen.

43. The reactor of claim 40, wherein the gas is provided to the reactor chamber at a flow rate of 100 SCCM to 10,000 SCCM for the oxygen containing gas, 5 SCCM to 1,000 SCCM for the halogen containing gas, and 10 SCCM to 5,000 SCCM of the hydrogen containing gas.

44. The reactor of claim 40, wherein the means for controlling the plasma potential includes a slotted conducting structure surrounding the plasma.

45. The reactor of claim 44, wherein the slotted conducting structure is electrically coupled to ground in the second mode.

46. A method for processing a semiconductor wafer comprising:

generating a plasma to produce charged particles and neutral species;

inducing bombardment of the semiconductor wafer by charged particles from the plasma at a first level for a first mode of processing;

limiting bombardment of the semiconductor wafer to a level substantially less than the first level for a second mode of processing; and

exposing the semiconductor wafer to neutral species from the plasma during the second mode at a desired level for processing;

wherein the semiconductor wafer is selectively processed using both the first and the second modes of processing.

47. The method of claim 46, wherein the plasma includes a halogen, oxygen, and

hydrogen.

48. The method of claim 47, wherein the halogen includes fluorine.

49. The method of claim 46, wherein generating the plasma includes flowing gas at a flow rate of 100 SCCM to 10,000 SCCM for an oxygen containing gas, 5 SCCM to 1,000 SCCM for a halogen containing gas, and 10 SCCM to 5,000 SCCM for a hydrogen containing gas.

50. The method of claim 47, wherein inducing bombardment of the semiconductor wafer by charged particles from the plasma at a first level includes surrounding the plasma with a slotted conducting structure.

51. The method of claim 50, wherein limiting bombardment of the semiconductor wafer to a level substantially less than the first level includes electrically coupling the slotted conducting structure to ground.

52. The method of claim 46, wherein inducing bombardment of the semiconductor wafer by charged particles from the plasma at a first level is performed for a period of 1 to 5 minutes.

53. The method of claim 46, comprising maintaining the semiconductor wafer at a temperature below about 100 degrees Celsius.

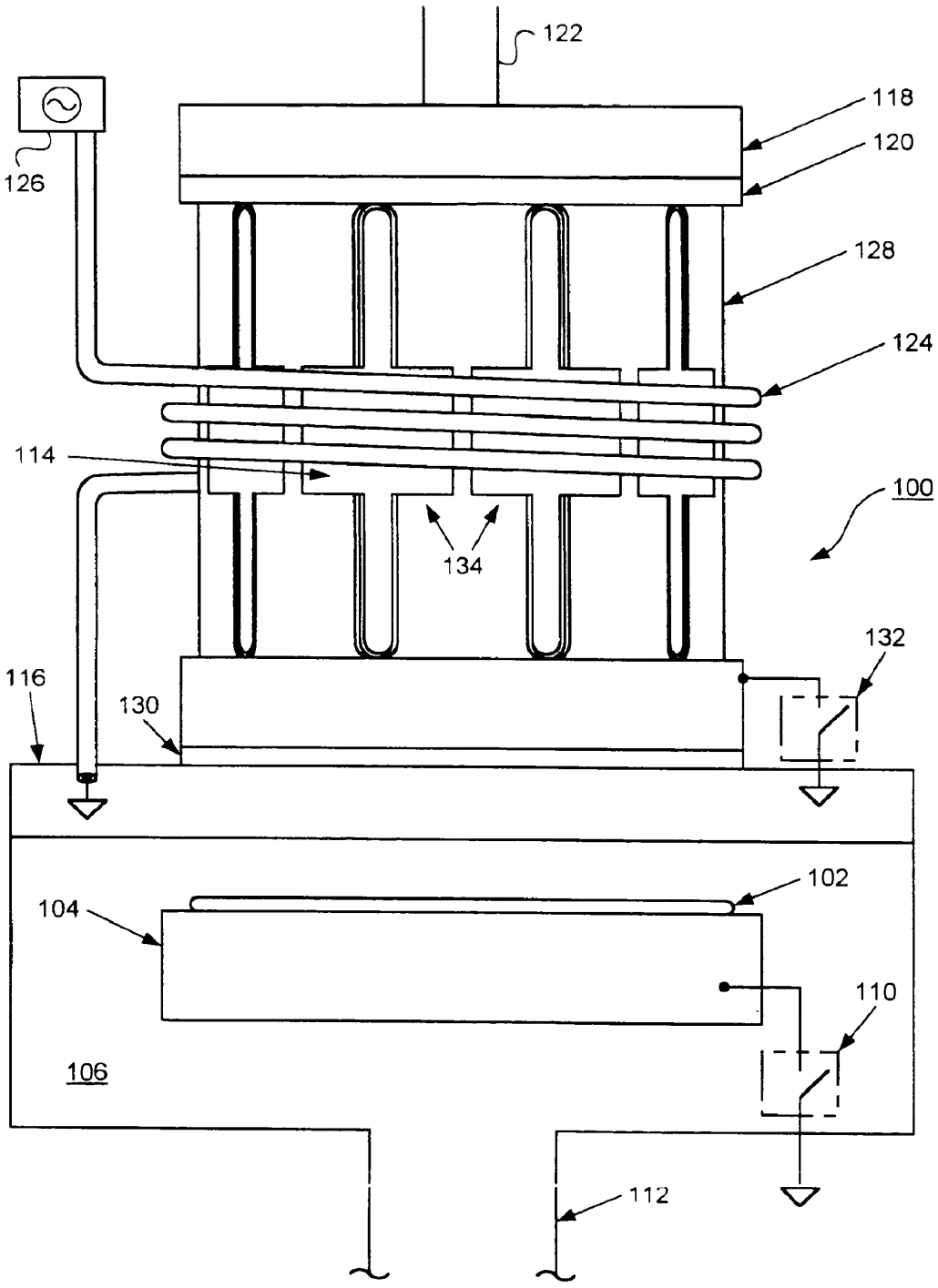
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Figure 1

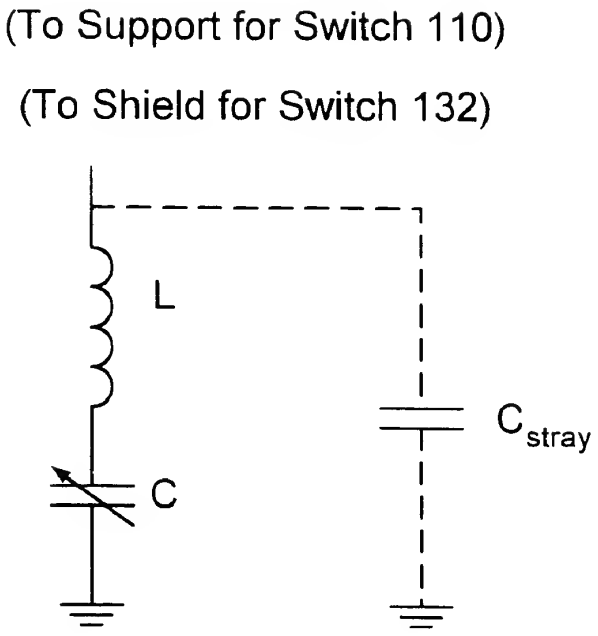

Figure 2

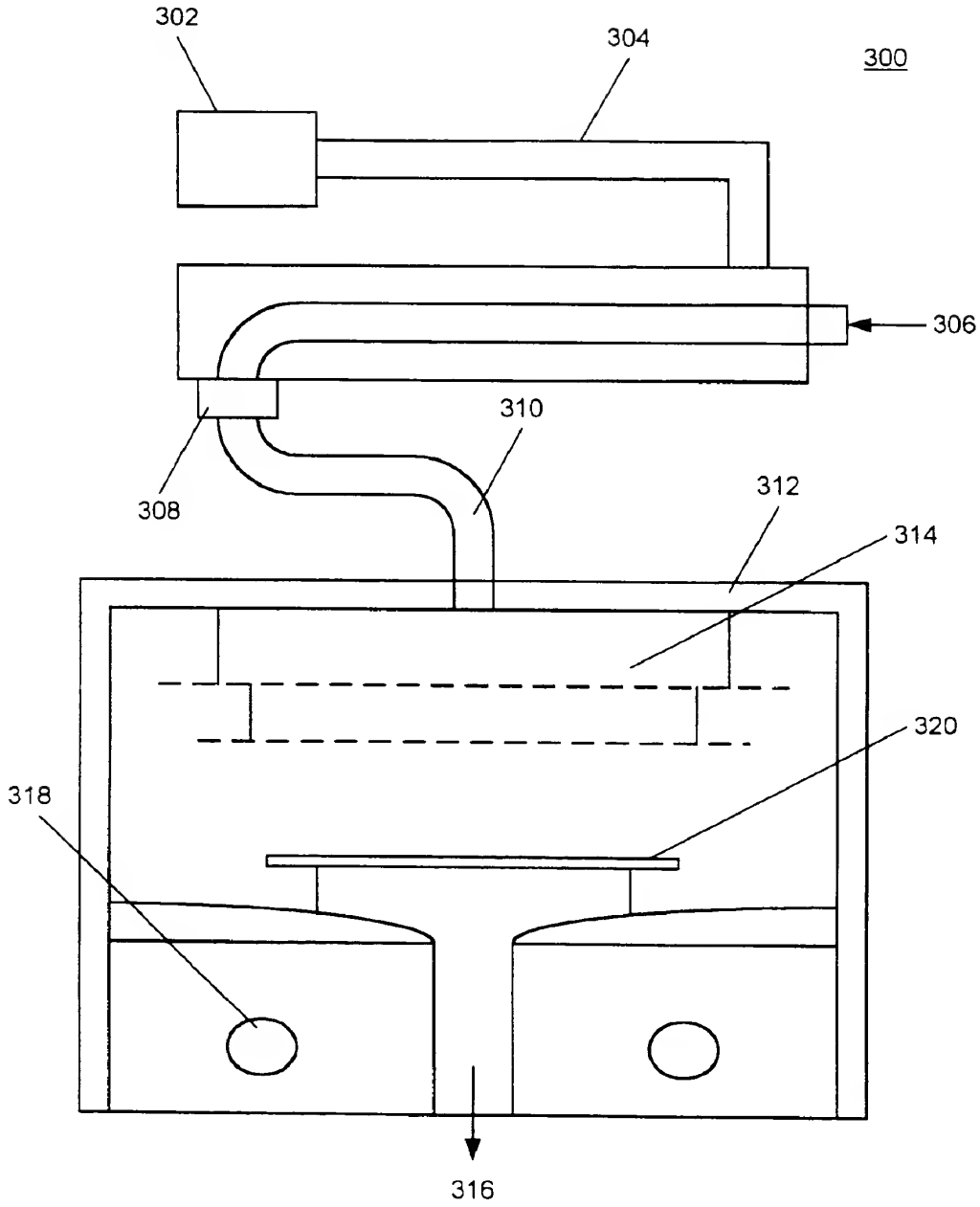

Figure 3

Process Step	Description	Time (Secs.)	RF Time (Secs.)	RF Delay (Secs.)	Power (Watts)	Pressure (Torr)	O_2 (SCCM)	Forming Gas (SCCM)	CF_4 (SCCM)	Temp. (°C)	Shield Switch 132	Support Switch 110
1	Stabilization	5	0	0	0	8	5,000	1,400	90	85	Open (Floating)	Closed (Grounded)
2	Crust Etch	85	75	10	800	1.1	1,500	1,400	90	85	Open (Floating)	Closed (Grounded)
3	Ashing	75	75	0	1,100	0.6	1,500	1,400	90	85	Closed (Grounded)	Open (Floating)
4	Post Process	5	0	0	0	8	5,000	0	0	85	Open (Floating)	Closed (Grounded)

Figure 4A

Process Step	Description	Time (Secs.)	RF Time (Secs.)	RF Delay (Secs.)	Power (Watts)	Pressure (Torr)	O_2 (SCCM)	Forming Gas (SCCM)	CF_4 (SCCM)	Temp. (°C)	Shield Switch 132	Support Switch 110
1	Stabilization	5	0	0	0	8	2,300	600	90	85	Open (Floating)	Closed (Grounded)
2	Crust Etch	115	105	10	1,000	1.1	2,300	600	90	85	Open (Floating)	Closed (Grounded)
3	Ashing	75	75	0	1,200	0.6	2,300	600	90	85	Closed (Grounded)	Open (Floating)
4	Post Process	5	0	0	0	8	5,000	0	0	85	Open (Floating)	Closed (Grounded)

Figure 4B

Process Step	Description	Time (Secs.)	RF Time (Secs.)	RF Delay (Secs.)	Power (Watts)	Pressure (Torr)	O_2 (SCCM)	Forming Gas (SCCM)	CF_4 (SCCM)	Temp. (°C)	Shield Switch 132	Support Switch 110
1	Stabilization	6	2	4	850	1.1	0	500	300	75	Open (Floating)	Closed (Grounded)
2	Polymer Etch	20	20	0	650	2.5	0	1,900	300	75	Open (Floating)	Closed (Grounded)
3	Bulk Resist Strip	46	46	0	1,150	0.6	3,000	0	150	75	Closed (Grounded)	Open (Floating)
4	Residue Removal	30	30	0	650	2.5	0	1,900	300	75	Open (Floating)	Closed (Grounded)
5	Post Process	5	0	0	0	1.1	3,500	0	0	75	Open (Floating)	Closed (Grounded)

Figure 5

Process Step	Description	Time (Secs.)	RF Time (Secs.)	RF Delay (Secs.)	Power (Watts)	Pressure (Torr)	O_2 (SCCM)	Forming Gas (SCCM)	NF_3 (SCCM)	Temp. (°C)	Shield Switch 132	Support Switch 110
1	Stabil zation	5	0	0	0	8	5,000	0	0	25	Open (Floating)	Closed (Grounded)
2	Etch	75	65	10	800	0.7	3,000	0	30	25	Open (Floating)	Closed (Grounded)
3	Post Process	5	0	0	0	8	5,000	0	0	25	Open (Floating)	Closed (Grounded)

FIGURE 6

Final Passivation strip and clean

Read	**Recipe 8**	**Recipe Name Gres 62**			
Step Number	*Step 1*	*Step 2*	*Step 3*	*Step 4*	*Step 5*
RF Time (Sec)	0	25	85	10	0
RF Delay (Sec)	2	2	2	2	2
RF Power (Watts)	0	950	1350	1200	0
Pressure (Torr)	1.1	1.1	0.6	2.5	1.1
GAS 1: SCCM	2500	300	3000	0	3000
GAS 2: SCCM	0	500	375	750	0
GAS 3: SCCM	0	0	0	4100	0
Temperature (C)	75	75	75	75	75
End Point	0	0	0	0	0
PIN/VAC/RFT%/SII	NNNNN	NNNNN	YNNNN	NNNNN	NNNNN
Go To Next Step	Y	Y	Y	Y	N

FIGURE 7

Vias clean

Read	Recipe	Recipe Name Gres 31			
Step Number	*Step 1*	*Step 2*	*Step 3*	*Step 4*	*Step 5*
RF Time (Sec)	0	70	0	0	0
RF Delay (Sec)	2	2	2	0	0
RF Power (Watts)	0	700	0	0	0
Pressure (Torr)	0.6	0.6	0.6	0	0
GAS 1: SCCM	0	3000	3000	0	0
GAS 2: SCCM	425	425	0	0	0
GAS 3: SCCM	4500	0	0	0	0
Temperature (C)	75	75	75	0	0
End Point	0	0	0	0	0
PIN/VAC/RFT%/SII	NNNNN	YNNNN	YNNNN	NNNNN	NNNNN
Go To Next Step	Y	Y	N	N	N

FIGURE 8

Oxinitride loss for passivation

Read	**Recipe**	**Recipe Name VAP01**			
Step Number	*Step 1*	*Step 2*	*Step 3*	*Step 4*	*Step 5*
RF Time (Sec)	25	0	0	0	0
RF Delay (Sec)	2	2	2	0	0
RF Power (Watts)	950	0	0	0	0
Pressure (Torr)	1.1	0.6	1.1	0	0
GAS 1: SCCM	10	3000	3000	0	0
GAS 2: SCCM	500	375	0	0	0
GAS 3: SCCM	0	0	0	0	0
Temperature (C)	75	75	75	0	0
End Point	0	0	0	0	0
PIN/VAC/RFT%/SII	NNNNN	YNNNN	YNNNN	NNNNN	NNNNN
Go To Next Step	Y	Y	N	N	N

FIGURE 9

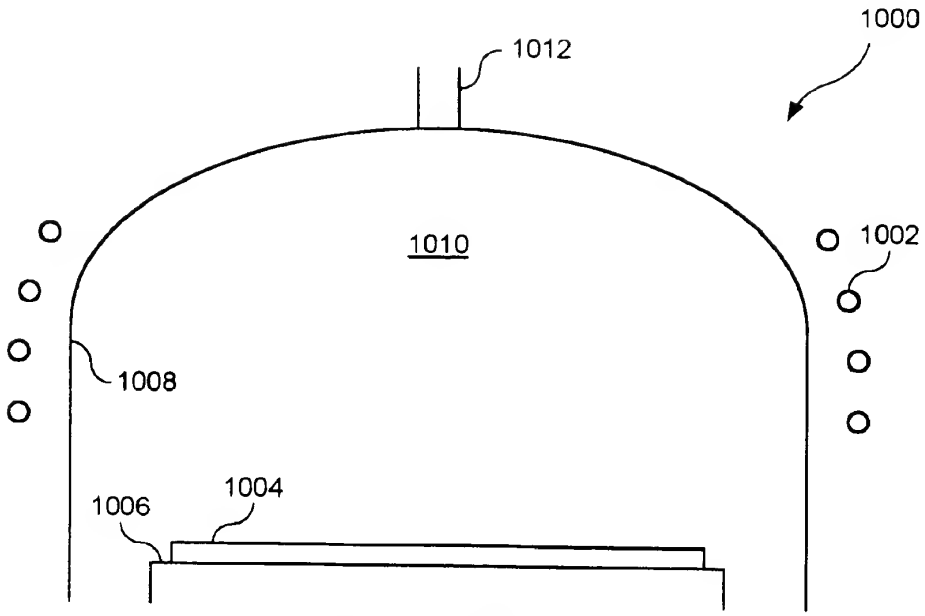

Figure 10A

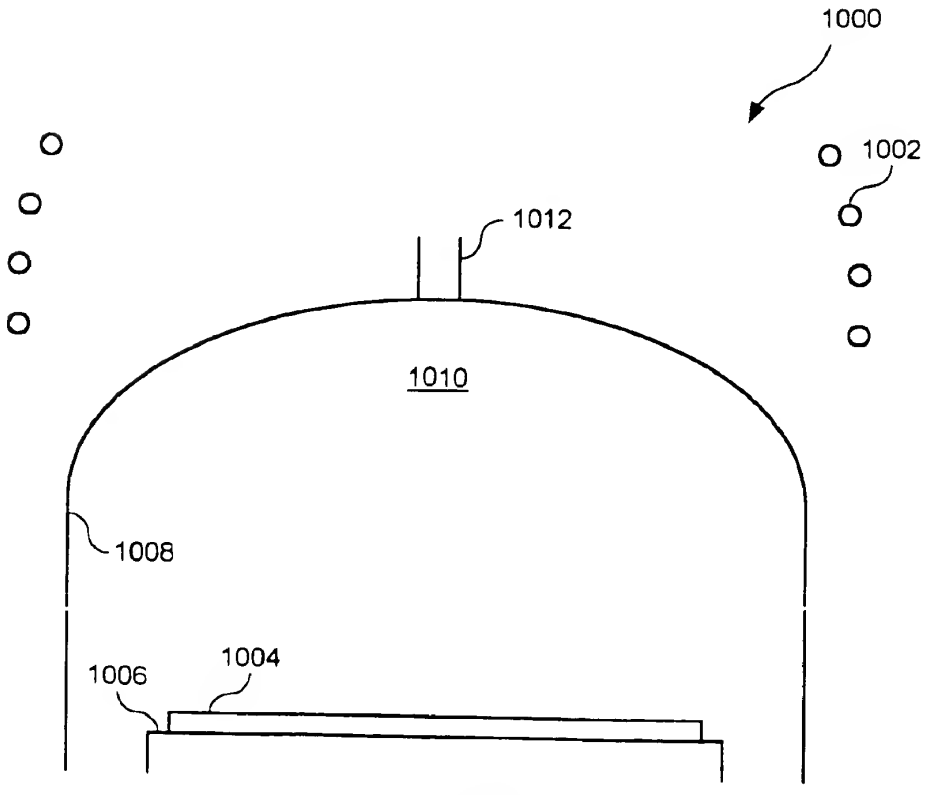

Figure 10B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/24557

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 21/00; B44C 1/22
US CL : 156/345; 216/67; 438/710, 720
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 156/345; 216/67, 69; 438/710, 714, 720, 725, 726

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,403,434 A (MOSLEHI) 04 April 1995, see entire document, especially the abstract.	1-53
A	US 5,403,436 A (FUJIMURA ET AL) 04 April 1995, see entire document.	1-53

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
16 FEBRUARY 1999	02 MAR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WILLIAM A. POWELL Telephone No. (703) 308-0661

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